REMARKS

Claims 1, 16, 19 and 20 have been amended. Support for the amendments can be found in the specification at page 14, lines 13-21, page 14, line 26 to page 15, line 1, and the figures of the present application. Claim 6 has been canceled solely to place the application in condition for allowance. Claims 1-5 and 7-22 remain pending in the application. Applicants reserve the right to pursue the original claims and other claims in this and other applications.

Presently, claims 1-3, 8-12, 14 and 20-22 stand rejected as being unpatentable over Yamagata in view of Miyazaki, claim 6 stands rejected as being unpatentable over Miyazaki, Yamagata, and Nakajima, claims 4, 5 and 7 stand rejected as being unpatentable over Miyazaki, Yamagata, and Morita, claim 13 stands rejected as being unpatentable over Miyazaki, Yamagata, and Negishi, claims 15, 16, 18 and 19 stand rejected as being unpatentable over Yamagata in view of Miyazaki and Kane and claim 17 stands rejected as being unpatentable over Miyazaki, Yamagata, Kane and Nakajima. All of the rejections were made under 35 U.S.C. § 103(a). The rejections are respectfully traversed.

Claim 1 recites a display unit for displaying an image and a drive unit for driving the display unit, the drive unit being connected by a plurality of signal lines. The "drive unit comprises a ladder resistor, impedance converters each having an input connected to an output of the ladder resistor, gray level voltage wires each connected to the output of the impedance converters, [and] gray level voltage selecting means selectively connecting said gray level voltage wires to said plurality of signal lines." According to claim 1, "said impedance converters have an offset voltage canceling unit for detecting and eliminating any offset voltage between input and output" (emphasis added). Applicants respectfully submit that the cited combinations fail to disclose, teach or suggest the subject matter of claim 1.

The feature that impedance converters "have an offset voltage canceling unit for detecting and eliminating any offset voltage between input and output" as claimed in the claim 1 configuration is simply not found in the cited combinations. Accordingly, for at least this reason, claim 1 is allowable over all of the cited combinations.

Moreover, as repeatedly argued, the cited combinations also fail to disclose, teach or suggest the limitation that "the number of said impedance converters matches the number of said gray level voltage wires and matches a number of a plurality of gray level voltage selectors of said gray level voltage selecting means connected to the gray level voltage wires." In addition and as illustrated in prior responses, Yamagata's system looks like: gray level voltage wires->impedance converters-> signal lines and Miyazaki's system looks like: ladder resistor ->impedance converters-> signal lines. These systems are different than the claimed invention. These are additional reasons why claim 1 is allowable over the cited combinations.

Applicants also submit that the cited combinations fail to disclose, teach or suggest "an image display apparatus having a drive unit including a ladder resistor, impedance converters each having an input connected to an output of a ladder resistor, said impedance converters detecting and eliminating any offset voltage, gray level voltage wires each connected to the output of the impedance converters, wherein the number of said impedance converters matches the number of said gray level voltage wires, and matches a number of a plurality of gray level voltage selectors connected to the gray level voltage wires in three separate phases when the analog image signal voltages are written onto the signal lines," as is recited in claim 16.

In addition, the cited combinations fail to disclose, teach or suggest a "drive circuit having a ladder resistor and a plurality of gray level voltage wires each connected through a plurality of impedance converters, respectively to an output of the ladder resistor, said impedance converters detecting and eliminating any offset voltage; said group of signal lines are connected to said gray level voltage wires via a gray level voltage selector; each gray level voltage wire is connected to the output of the impedance converters, respectively, wherein the number of said impedance converters matches the number of said gray level voltage wires; at least the display pixels, the group of signal lines, the gray level voltage selector and the gray level voltage wires are provided over the same substrate; and wherein the analog image signal voltages are written in three separate phases when the analog image signal voltages are to be written onto the signal lines," as is recited in claim 19.

Similarly, the cited references do not teach or suggest an image display terminal comprising a "drive circuit [having] a ladder resistor and a plurality of gray level voltage wires each connected through a plurality of impedance converters, respectively to an output of the ladder resistor; said group of signal lines are connected to the gray level voltage wires via a gray level voltage selector; each of said gray level voltage wires connected to the output of the impedance converters, respectively, wherein the number of said impedance converters matches the number of said gray level voltage wires, wherein said impedance converters have an offset voltage canceling unit for detecting and eliminating any offset voltage between input and output; and at least the display pixels, the group of signal lines, the gray level voltage selector and the gray level voltage wires are provided over a single substrate," as recited in claim 20.

As such, the cited combinations fail to disclose, teach or suggest all of the limitations of claims 1, 16, 19 and 20. Claims 2-5 and 7-15 and 22 depend from claim 1 and are allowable along with claim 1. Claims 17-18 depend from claim 16 and are allowable along with claim 16. Claim 21 depends from claim 20 and is allowable along with claim 20. Accordingly, the rejections should be withdrawn and the claims allowed.

In view of the above, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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